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((((CONCURRENT$4 OR SIMULTANEOUS$3 OR PARALLEL$7) NEAR8 EXECUT$3 AND (FETCH$5 OR PREFETCH$5) AND BRANCH$5 NEAR10 DECOD$4 AND TAKEN AND (INHIBIT$4 OR HALT$4 OR CANCEL$5 OR SUSPEND$3 OR SUSPENSION$1) NEAR8 (INSTRUCTION$1 OR MICROINSTRUCTION$1 OR MACROINSTRUCTION$1) AND IDENTIF$7).CLM.).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	1

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Search History

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	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L36	((concurrent$4 or simultaneous$3 or parallel$7) near8 execut$3 and (fetch$5 or prefetch$5) and branch$5 near10 decod$4 and taken and (inhibit$4 or halt$4 or cancel$5 or suspend$3 or suspension$1) near8 (instruction$1 or microinstruction$1 or macroinstruction$1) and identif$7).clm.	1	L36
L35	((fetch$5 or prefetch$5) and branch$5 near10 decod$4 and taken and (inhibit$4 or halt$4 or cancel$5 or suspend$3 or suspension$1) near8 (instruction$1 or microinstruction$1 or macroinstruction$1) and identif$7).clm.	3	L35
L34	L33 not 19	3	L34
L33	L32 and 18	356	L33
L32	L31 and 14	426	L32
L31	(inhibit$4 or halt$4 or cancel$5 or suspend$3 or suspension$1) near8 (instruction$1 or microinstruction$1 or macroinstruction$1)	14105	L31
	DB=PGPB,USPT; PLUR=YES; OP=OR		
L30	110 and 115	12	L30
L29	110 and 114	68	L29
L28	110 and 113	7	L28
L27	110 and 112	77	L27
L26	110 and 111	228	L26
L25	19 and 115	16	L25
L24	19 and 114	83	L24
L23	19 and 113	12	L23
L22	19 and 112	100	L22
L21	19 and 111	292	L21
L20	17 and 115	18	L20
L19	17 and 114	95	L19
L18	17 and 113	15	L18
L17	17 and 112	113	L17
L16	17 and 111	340	L16
L15	(711/213)[CCLS]	457	L15
L14	(712/23,41)[CCLS]	841	L14
L13	(712/245-248)[CCLS]	794	L13
L12	(712/23-43, 208-240)![CCLS]	3391	L12
L11	(712/2-300)[CCLS]	12464	L11
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L10	L9 and branch$3 near8 decod$3	264	L10
L9	L8 and 17	353	L9
L8	(identif$6 or id) near8 (instruction$1 or microinstruction$1 or macroinstruction$1)	36602	L8

L7	L6 and l4	420	L7
L6	L5	13605	L6
L5	(inhibit$4 or halt$4 or cancel$5 or suspend$3 or syspension$1) near8 (instruction$1 or microinstruction$1 or macroinstruction$1)	13605	L5
L4	L3 and l2	1087	L4
L3	(fetch$5 or prefetch$5) and (branch$4) near7 (predict$5 or speculat$5) near25 taken	1747	L3
L2	(concurrent$4 or simultaneous$3 or parallel$7) near8 execut$3	66419	L2
L1	(fetch$5 or prefetch$5) and (branch$4) near7 (predict$5 or speculat$5)	4203	L1

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                                                      Computers, IEEE Transactions on
                                                      Volume 55, Issue 3, March 2006 Page(s):281 - 291
                                                      Digital Object Identifier 10.1109/TC.2006.32

                                                      Summary: Conventional front-end designs attempt to maximize the number of "in-flight" instruction
                                                      However, branch mispredictions cause the processor to fetch useless instructions that are eventua
                                                      increasing front-end energy and .....

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                                              ☐   2. **Power-aware control speculation through selective throttling**
                                                      Aragon, J.L.; Gonzalez, J.; Gonzalez, A.;
                                                      High-Performance Computer Architecture, 2003. HPCA-9 2003. Proceedings. The Ninth Internatio
                                                      8-12 Feb. 2003 Page(s):103 - 112
                                                      Digital Object Identifier 10.1109/HPCA.2003.1183528

                                                      Summary: With the constant advances in technology that lead to the increasing of the transistor cc
                                                      frequency, power dissipation is becoming one of the major issues in high-performance processors.
                                                      increase their clock frequenc.....

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